


TDS 3/4/04 10/723 547 1/2

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18
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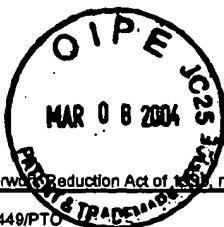
Title of Invention	A Vertical Replacement-Gate Junction Field-Effect Transistor																																																																																																																																					
<p>Application Number: 10/723547 </p> <p>Confirmation Number: 9745</p> <p>First Named Applicant: Samir Chaudhry</p> <p>Attorney Docket Number: 075903-285</p> <p>Art Unit: 2811</p> <p>Search string: (5367184 or 5599724 or 5414289 or 5576238 or 5668391 or 5744846 or 6297531 or 4366495 or 4455565 or 4587713 or 4683643 or 4786953 or 4837606 or 5342797 or 6027975 or 6072216 or 6133099 or 6197641 or 5866925 or 5889298).pn.</p> <p>US Patent Documents</p> <p>Note: Applicant is not required to submit a paper copy of cited US Patent Documents</p> <table border="1"><thead><tr><th>init</th><th>Cite.No.</th><th>Patent No.</th><th>Date</th><th>Patentee</th><th>Kind</th><th>Class</th><th>Subclass</th></tr></thead><tbody><tr><td><input checked="" type="checkbox"/></td><td>1</td><td>5367184</td><td>1994-11-22</td><td>Chantre</td><td></td><td></td><td></td></tr><tr><td><input checked="" type="checkbox"/></td><td>2</td><td>5599724</td><td>1997-02-04</td><td>Yoshida</td><td></td><td></td><td></td></tr><tr><td><input type="checkbox"/></td><td>3</td><td>5414289</td><td>1995-05-09</td><td>Fitch, et al</td><td></td><td></td><td></td></tr><tr><td><input type="checkbox"/></td><td>4</td><td>5576238</td><td>1996-11-19</td><td>Fu</td><td></td><td></td><td></td></tr><tr><td><input type="checkbox"/></td><td>5</td><td>5668391</td><td>1997-09-16</td><td>Kim, et al</td><td></td><td></td><td></td></tr><tr><td><input type="checkbox"/></td><td>6</td><td>5744846</td><td>1998-04-28</td><td>Batra, et al</td><td></td><td></td><td></td></tr><tr><td><input type="checkbox"/></td><td>7</td><td>6297531</td><td>2001-10-02</td><td>Armacost, et al</td><td></td><td></td><td></td></tr><tr><td><input type="checkbox"/></td><td>8</td><td>4366495</td><td>1982-12-28</td><td>Goodman, et al</td><td></td><td></td><td></td></tr><tr><td><input type="checkbox"/></td><td>9</td><td>4455565</td><td>1984-06-19</td><td>Goodman, et al</td><td></td><td></td><td></td></tr><tr><td><input type="checkbox"/></td><td>10</td><td>4587713</td><td>1986-05-13</td><td>Goodman, et al</td><td></td><td></td><td></td></tr><tr><td><input type="checkbox"/></td><td>11</td><td>4683643</td><td>1987-08-04</td><td>Nakajima, et al</td><td></td><td></td><td></td></tr><tr><td><input type="checkbox"/></td><td>12</td><td>4786953</td><td>1988-11-22</td><td>Morie, et al</td><td></td><td></td><td></td></tr><tr><td><input type="checkbox"/></td><td>13</td><td>4837606</td><td>1989-06-06</td><td>Goodman, et al</td><td></td><td></td><td></td></tr><tr><td><input checked="" type="checkbox"/></td><td>14</td><td>5342797</td><td>1994-08-30</td><td>Sapp, et al</td><td></td><td></td><td></td></tr><tr><td><input checked="" type="checkbox"/></td><td>15</td><td>6027975</td><td>2000-02-22</td><td>Hergenrother, et al</td><td></td><td></td><td></td></tr></tbody></table>							init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass	<input checked="" type="checkbox"/>	1	5367184	1994-11-22	Chantre				<input checked="" type="checkbox"/>	2	5599724	1997-02-04	Yoshida				<input type="checkbox"/>	3	5414289	1995-05-09	Fitch, et al				<input type="checkbox"/>	4	5576238	1996-11-19	Fu				<input type="checkbox"/>	5	5668391	1997-09-16	Kim, et al				<input type="checkbox"/>	6	5744846	1998-04-28	Batra, et al				<input type="checkbox"/>	7	6297531	2001-10-02	Armacost, et al				<input type="checkbox"/>	8	4366495	1982-12-28	Goodman, et al				<input type="checkbox"/>	9	4455565	1984-06-19	Goodman, et al				<input type="checkbox"/>	10	4587713	1986-05-13	Goodman, et al				<input type="checkbox"/>	11	4683643	1987-08-04	Nakajima, et al				<input type="checkbox"/>	12	4786953	1988-11-22	Morie, et al				<input type="checkbox"/>	13	4837606	1989-06-06	Goodman, et al				<input checked="" type="checkbox"/>	14	5342797	1994-08-30	Sapp, et al				<input checked="" type="checkbox"/>	15	6027975	2000-02-22	Hergenrother, et al			
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MT	16	6072216	2000-06-06	Williams, et al
↑	17	6133099	2000-10-17	Sawada
↓	18	6197641	2001-03-06	Hergenrother, et al
↓	19	5866925	1999-02-02	Zolper, et al
MT	20	5889298	1999-03-30	Plumton, et al

Signature

Examiner Name	Date
Michael Trish	9/28/04



IDS 3/8/04

PTO/SB/08B (08-03)

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known			
		Application Number	10/723,547		
		Filing Date	11/26/2003		
		First Named Inventor	Samir Chaudhry		
		Art Unit	2811 2822		
		Examiner Name	Unassigned		
Sheet	1	of	1	Attorney Docket Number	Chaudhry 26-19-9-13-6/075903-285

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
MS	1	DUDEK, ET AL, "Lithography-Independent Nanometer Silicon MOSFET's on Insulator", IEEE Transactions on Electron Devices, Vol. 43, No. 10, October 1996, pp. 1626-1631.	
MT	2	RISCH, ET AL, "Vertical MOS Transistors with 70 nm Channel Length", IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996, pp. 1495-1498.	
MT	3	TAKATO, ET AL, "Impact of Surrounding Gate Transistor (SGT) for Ultra-High-Density LSI's", IEEE Transactions on Electron Devices, Vol. 38, No. 3, March 1991, pp. 573-577.	
MS	4	TAKATO, ET AL, "High Performance CMOS Surrounding Gate Transistor (SGT) for Ultra High Density LSI's", IEDM 1988, pp. 222-225.	
MT	5	HERGENROTHER, ET AL, "The Vertical Replacement-Gate (VRG) MOSFET: A 50-nm Vertical MOSFET with Lithography-Independent Gate Length", Technical Digest of IEDM, 1999, pp. 75-78.	
MT	6	OH, ET AL, "50 nm Vertical Replacement-Gate (VRG) pMOSFET's", IEEE 2000, 4 pages	
MT	7	HERGENROTHER, ET AL, "The Vertical Replacement-Gate (VRG) MOSFET: A High Performance Vertical MOSFET with Lithography-Independent Critical Dimensions", no publication information apparent from document, 1 pages.	
MT	8	MONROE, ET AL, "The Vertical Replacement-Gate (VRG) Process for Scalable, General-purpose Complementary Logic", Paper 7.5, pp. 1-7, date and publication information unknown.	

Examiner Signature	Michael Trinch	Date Considered	9/28/04
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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